

**The invention claimed is:**

- 1 1: An apparatus which comprises:  
2 a multi-core processor and  
3 at least one test control mechanism;  
4 said multi-core processor and said test control mechanism having a configuration  
5 so as to allow testing of said multi-core processor.
- 1 2: The apparatus of claim 1, wherein said multi-core processor comprises at least two  
2 processor cores and at least one circuit comprising non-processor core logic.
- 1 3: The apparatus of claim 2, wherein said multi-core processor and said test control  
2 mechanism having a configuration so as to allow testing of at least two processor cores of  
3 said multi-core processor.
- 1 4: The apparatus of claim 2, wherein said at least one test control mechanism  
2 respectively comprises at least one test access port controller (TAPC) and a plurality of  
3 distributed data and control registers; wherein said plurality of distributed data and  
4 control registers are located both within said at least two processor cores and within said  
5 at least one circuit comprising non-core logic.
- 1 5: The apparatus of claim 4, wherein said at least one test control mechanism is  
2 substantially compliant with the IEEE 1149.1 specification.
- 1 6: The apparatus of claim 4, wherein said at least one test access port controller (TAPC)  
2 is located within said at least two processor cores.

1 7: The apparatus of claim 4, wherein said at least one test access port controller (TAPC)  
2 and at least one of said plurality of distributed data and control registers are coupled via  
3 an Integrated Test Bus (ITB).

1 8: The apparatus of claim 4, wherein said distributed test control mechanism is  
2 controllable, at least in part, by one of said at least one test access port controller (TAPC).

1 9: The apparatus of claim 8, wherein which of said at least one test access port  
2 controllers (TAPCs) controls said distributed test control mechanism is dynamically  
3 selectable during operation.

1 10: The apparatus of claim 2, wherein at least one of the said at least two processor cores  
2 comprises one test access port (TAP) which includes one test access port controller  
3 (TAPC), and a plurality of distributed data and control registers.

1 11: The apparatus of claim 10, wherein said test control mechanism and said at least two  
2 processor cores are coupled so as to provide multiple coupling arrangements, said  
3 multiple coupling arrangements being dynamically selectable during operation.

1 12: The apparatus of claim 11, wherein said multiple coupling arrangements are selected  
2 from a group consisting essentially of coupling said test access ports substantially in  
3 series, coupling said test access ports substantially in parallel and coupling said test  
4 access ports for substantially independent operation.

1 13: The apparatus of claim 10, wherein said at least one test control mechanism is  
2 arranged to allow at least one of said at least two processor cores' said one test access  
3 port (TAP) to be externally visible from said multi-core processor.

1 14: The apparatus of claim 13, wherein said at least one test control mechanism is  
2 arranged to allow only one of said at least two processor cores' said one test access port  
3 (TAP) to be externally visible from said multi-core processor.

1 15: The apparatus of claim 13, wherein said at least one test control mechanism is  
2 arranged to allow the selection of which at least one of said at least two processor cores'  
3 said one test access port (TAP) is externally visible from said multi-core processor to  
4 occur dynamically.

1 16: The apparatus of claim 10, wherein said at least one test control mechanism is  
2 coupled to produce during operation an error signal if the output signals of said at least  
3 two processor cores' said one test access port (TAP) are not substantially equivalent.

1 17: The apparatus of claim 2, wherein said at least one test control mechanism, said at  
2 least one processor core and said at least one circuit comprising non-processor core logic  
3 are further coupled so as to allow testing of said at least one circuit comprising non-  
4 processor core logic.

1 18: A system which comprises:

2 a computing platform, including:

3 a memory to store instructions;

4 a multi-core processor to process instructions which includes:

5 a plurality of processor cores;

6 at least one circuit comprising non-processor core logic and

7 a test control mechanism;

8           said multi-core processor and said test control mechanism having a configuration  
9   so as to allow testing of said plurality of processor cores.

1   19: The system of claim 18, wherein said multi-core processor and said test control  
2   mechanism are further arranged so as to allow testing of said at least one circuit  
3   comprising non-processor core logic.

1   20: The system of claim 18, wherein said test control mechanism comprises at least one  
2   test access port controller (TAPC) and a plurality of distributed data and control registers;  
3   wherein said plurality of distributed data and control registers are located both within said  
4   plurality of processor cores and within said at least one circuit comprising non-core logic.

1   21: The system of claim 20, wherein said at least one test control mechanism is  
2   substantially compliant with the IEEE 1149.1 specification.

1   22: The system of claim 20, wherein said at least one test access port controller (TAPC)  
2   is located within said plurality of two processor cores.

1   23: The system of claim 20, wherein said at least one test access port controller (TAPC)  
2   and at least one of said a plurality of distributed data and control registers are coupled via  
3   an Integrated Test Bus (ITB).

1   24: The system of claim 20, wherein said distributed test control mechanism is  
2   controlled, at least in part, by one of said at least one test access port controller (TAPC).

1 25: The system of claim 24, wherein which of said at least one test access port  
2 controllers (TAPCs) controls said distributed test control mechanism is be dynamically  
3 selected during operation.

1 26: The system of claim 18, wherein each of the said at least two processor cores  
2 comprises one test access port (TAP) which includes one test access port controller  
3 (TAPC), and a plurality of distributed data and control registers.

1 27: The system of claim 26, wherein said test control mechanism and said at least two  
2 processor cores are coupled so as to provide multiple coupling arrangements, said  
3 multiple coupling arrangements being dynamically selected during operation.

1 28: The system of claim 27, wherein said multiple coupling configurations are selected  
2 from a group consisting essentially of coupling said test access ports substantially in  
3 series, coupling said test access ports substantially in parallel, and coupling said test  
4 access ports for substantially independent operation.

1 29: The system of claim 26, wherein said test control mechanism is coupled to produce,  
2 during operation, a signal that indicates whether the output signals of said at least two  
3 processor cores' said one test access port (TAP) are equivalent or substantially  
4 equivalent.

1 30: A method, comprising:  
2 providing an indicator to identify a desired testing option;  
3 based upon said desired testing option, dynamically routing signals between a  
4 plurality test access ports (TAPs);

5 wherein said plurality test access ports (TAPs) are part of a multi-core processor;  
6 said multi-processor core including a plurality of processor cores.

1 31: The method of claim 30, wherein the routing of said signals is selected from a group  
2 consisting essentially of coupling said test access ports substantially in series, coupling  
3 said test access ports substantially in parallel, and coupling said test access ports for  
4 substantially independent operation.

1 32: The method of claim 31, wherein providing an indicator to identify a desired testing  
2 option comprises storing control information in a register.

1 33: The method of claim 32, wherein storing control information in a register comprises  
2 shifting said data into the register in a serial fashion.

1 34: The method of claim 32, wherein storing control information in a register comprises  
2 a step in compliance with the operation of test data registers as described in the IEEE  
3 1149.1 specification.

1 35: The method of claim 30, wherein dynamically routing signals between a plurality of  
2 test access ports (TAPs) comprises dynamically routing signals between a plurality of test  
3 access port controllers (TAPCs) and a plurality of distributed data and control registers.

1 36: The method of claim 30, wherein dynamically routing signals between a plurality of  
2 test access ports (TAPs) comprises only altering the routing of signals external to said  
3 plurality of processor cores.

- 1 37: The method of claim 30, which further comprises producing a signal that indicates
- 2 whether the output signals of said at least two processor cores' said one test access port
- 3 (TAP) are equivalent or substantially equivalent